Total No. of Questions : 8] *[Total No. of Printed Pages :2*

Roll No .....

EC-605

B.E. VI Semester
Examination, June 2017
VLSI Circuits and Systems

Time : Three Hours

Maximum Marks : 70

Note: i) Answer any five questions.
ii) All questions carry equal marks.

1. a) Explain the VLSI design flow with the help of y-chart.
   b) Discuss the concepts of regularity, modularity and locality in VLSI design.

2. a) Design the following circuits using transmission gates
      i) Half adder
      ii) D flip-flop.
   b) What do you understand by the term state diagram? How will you obtain the state table from it?

3. a) State the difference between Mealy and Moore machine. Give simple example and draw the state transition diagram for the two.
   b) A sequential circuit has 2D ff's A and B an input x and output Y is specified by the following next state and output equations.
      $A(t+1) = Ax + Bx$
      $B(t+1) = A'x$
      $Y = (A+B)x'$
      Derive the state table and the state diagram.

4. a) Explain secondary state assignment in sequential machines.
   b) Discuss the minimum requirement of pulse mode and fundamental mode sequential machine.

5. a) Find the hazard in network which realizes the function:
      $y = (x_1 + x_2)(x'_2 + x_3)$
      Eliminate it.
   b) How does the state assignment for synchronous machine differ from that of asynchronous machine?

6. a) Define Path Sensitization. Explain heuristic procedure for sensitizing paths with the help of an example.
   b) Draw an ASM chart for a comparator and explain it.

7. a) What do you understand by "Algorithmic State machine"? What is the concept of hardware and firmware algorithm?
   b) Explain different fault models in detail.

8. a) What is FPGA? Describe various types of FPGA with diagram.
   b) Implement the following two functions using PLA and PAL.
      i) F1 = BA + C'b'A + CB'a'
      ii) F2 = C'b'A + CBA.

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